BUR920010156US2

AMENDMENTS TO THE SPECIFICATION:

On page 1 at the first line following the title, please amend the following section:

Reference to Related Application

This application is a divisional of Application No. 10/248,452, filed January 21, 2003, now issued as U.S. Patent No. 6,674,168.

Please amend the following paragraphs of the specification:

4. Currently, integrated circuit BEOL (back end of the line) semiconductor processing rework processes are used for both ASIC (Application Specific Integrated Circuit) design and normal production. These rework processes have been developed for both and copper multi-level-metal wiring and are generally employed to correct yield or problems or a photomask error. Such rework processes enable QTAT (quicker turn around time) design verification and save integrated circuit fabrication costs. An example of a process is given in U.S. Patent Number 6,332,988, the complete disclosure of which is incorporated by reference, wherein a process for reworking electroplated solder bump is disclosed.

5. The introduction of copper and low dielectric (k) technologies presents the for additional rework process definition because the physical and chemical properties low k dielectric materials differ significantly from silicon dioxide, and therefore are not to the same rework procedures. Such rework processes must integrate with POR (process of ~~record back end of line~~ record) BEOL processing sequences, maintain planarity throughout rework process, remove multiple thin films including Si_3N_4, low k organic dielectrics, copper, liner materials, and stop on the top of the dielectric and tungsten interconnect region residing the electronically active

devices such as transistors (typically called the front end). This dielectric is typically Boron-doped SiO2 or "BPSG" (Boron Phosphorous Silicate Glass), an electrical conductor fabricated of tungsten damascene is typically utilized so this can be abbreviated "BPSG/W". Some conventional processes teach methods for a defective SiLK® layer caused by improper coating such as for a photoresist process. However, these conventional processes do not address rework of the final metal in addition to the dielectric BEOL.

9. There is provided, according to one aspect of the invention, a method of reworking BEOL ~~(back-end-of-a-processing-lines)~~ interconnect levels of damascene metallurgy, wherein each of the levels comprise a line portion and a via portion embedded in multiple dielectric layers. The method comprises sequentially removing the interconnect levels by selectively removing the multiple dielectric layers beginning with an uppermost dielectric layer. Then, the line and via portions of the interconnect levels are exposed. Next, the exposed line and via portions of the interconnect levels are coplanarized. Finally, the removed interconnect levels are replaced with full interconnect levels of damascene metallurgy.

72. Figures 6 through 10 describe the sequence relating to the method for practicing this embodiment according to the present invention. As shown in Figure 6, the first step involves providing a substrate 210l (such as a silicon substrate) having ~~BEOL~~ FEOL (front-end-of-line) devices, and one or more BEOL metallization levels 201, 202 fabricated thereon. The integrated circuit device 200, as shown, specifically comprises a first insulator layer 220 comprising a low dielectric constant material (low k dielectric), such as SiLK®, FLARE®, and traditional materials as silicon dioxide, fluorinated silicon dioxide (FSG), and microporous glasses such as

Nanoglass®, as well as Black Diamond, Coral, and Xerogel.

81. As shown in Figure 11, the first step involves providing a substrate 310 (such as a silicon substrate) having ~~BEOL~~ FEOL (front-end-of-line) devices, and one or more BEOL metallization levels 301, 302, 303, 304 fabricated thereon. The integrated circuit device 300, as shown, specifically comprises a first insulator layer 320 comprising a low dielectric constant material (low k dielectric), such as SiLK®, FLARE®, and traditional materials such as silicon dioxide, silicon dioxide (FSG) and microporous glasses such as Nanoglass®, as well as Black Diamond, Coral, and Xerogel.

103. Figure 30 illustrates a flow diagram of a rework process according to the present invention. The method of reworking BEOL ~~(back-end-of-a-processing-line)~~ interconnect levels of damascene metallurgy comprises first forming 2000 a first interconnect level over a substrate, which further comprises depositing 2010 a first dielectric layer over the substrate, laying 2020 a second dielectric layer over the first dielectric layer, and forming 2030 line and via regions in the first and second dielectric layers, wherein the first dielectric layer comprises a lower dielectric constant material than the first dielectric layer. Then, a plurality of interconnect levels are formed 2040 over the first interconnect level. Next, selective interconnect levels are removed 2050 beginning with an uppermost interconnect level. Finally, the removed interconnect levels are replaced 2060 with new interconnect levels.